REMARKS

Claims 8, 12, 15 and 19 have been amended. Claims 8-21 are still pending. There are no new claims. Claims 1-7 have been canceled prior to the current response.

Claims 8-13 and 15-20 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,963,810 issued to Gardner, et al. (hereinafter "Gardner") in view of U.S. Patent No. 4,015,281 issued to Nagata, et al. (hereinafter "Nagata"), and U.S. Patent No. 5,990,516 issued to Momose, et al. (hereinafter "Momose"). The Applicant respectfully disagrees for the following reasons.

Claims 8 and 15 are prima facie not obvious over the cited references because combined the cited references fail to teach or suggest every element of the claims. In regard to claims 8 and 15, it has been requested that they be amended to include the additional element that "the first and second dielectric materials being scalable for a feature size technology". None of the cited references disclose a transistor device having at least two dielectrical layers with different dielectric constants being scaled for a given technology. Gardner discloses forming a layer of nitride over a substrate and then forming a high permittivity gate insulating layer over the nitride layer. The only advantage added by this lower nitride layer as disclosed by Gardner is that it provides a more receptive surface in which the high permittivity gate insulating layer can be disposed. Gardner, col. 6, lines 43-49. A dielectric constant of the high permitivity layer or the nitride layer is not specified by Gardner. Gardner teaches selecting the thickness of the high permitivity layer based on obtaining desired properties and reliability, but does not teach scaling to a feature size technology. Gardner col. 3, line 66-col. 4, line 10. The nitride layer is restricted to a range of 5 to 15Å. Gardner col. 5, lines 48-50. Thus it cannot be said that Gardner

discloses a second dielectric material having a second dielectric constant different from the first dielectric constant or scalable for a feature size technology. See claim 8, lines 4 and 5.

Momose discloses a single layer gate dielectric that is less than 1/3 of the length of a gate. However, Momose's teachings are limited to gates of length less than 0.3μm and to gate insulating films of less than 2.5 nm. See Momose col. 2, lines 52-58. Thus, Momose does not teach a first and second dielectrical material, the combination of whose thickness is less than 1/3 of the length of the transistor gate, in a manner in which it may be scaled for technology that requires a transistor gate length of greater than 0.3 μm or a gate insulating film of greater than 2.5 nm.

Nagata does not teach any relationship between dielectric layers in terms of their dielectric constants. Nagata teaches only varying the thickness of two dielectric layers so that either may predominate over the other to selectively induce electrons or holes in the surface of the substrate. Nagata col. 2, lines 46-64. Therefore, nothing in the cited references teaches or suggests dielectric layers with different constants or varying the dielectric layers of the gate in terms of their constants or thicknesses to scale them for a feature size technology. Accordingly, reconsideration and withdrawal of the rejection of claim 8 and 15 are requested.

In regard to claims 9 and 16, Gardner does not specify a dielectric constant for the nitride layer or the high permitivity layer. Thus, Gardner cannot be said to disclose a second dielectric layer having a greater dielectric constant than the first dielectric material. Neither Nagata nor Momose teach a second dielectric layer having a dielectric constant greater than the first as discussed in regard to claim 8 and 15 above. Further, claims 9 and 16 incorporated the limitations of claims 8 and 15 respectively and are not obvious at least for the reasons mentioned in regard to claims 8 and 15. Accordingly, reconsideration and withdrawal of the rejection of claims 9 and 16 are requested.

In regard to claims 12 and 19, none of the cited references teach or suggest the first gate dielectric material being selected from one of HfO_2 or ZrO_2. Accordingly, reconsideration and withdrawal of the rejection of claims 12 and 19 are requested.

In regard to claims 10, 11 and 13, these claims depend from claim 8 and incorporate the limitations thereof and thus, are not obvious, at least for the reasons given in regard to claim 8. Accordingly, reconsideration and withdrawal of the rejection of claims 10, 11 and 13 are requested.

In regard to claims 17, 18 and 20, these claims depend from claim 15 and incorporate the limitations thereof and thus, are not obvious, at least for the reasons given in regard to claim 15. Accordingly, reconsideration and withdrawal of the rejection of claims 17, 18 and 20 are requested.

Claims 14 and 21 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Gardner in view of Nagata and Momose, and in further view of U.S. Patent No. 5,258,645 issued to Sato (hereinafter "Sato"). These claims depend from claims 8 and 15, respectively, and thus incorporate the limitations of those claims. Therefore, claims 14 and 21 are not obvious, at least for the reasons given in regard to claims 8 and 15. Accordingly, reconsideration and withdrawal of the rejection of claims 14 and 21 are requested.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending, namely claims 8-21 patentably define the subject invention over the prior art of record, and are in condition for allowance and such action as earnestly solicited at the earliest possible date. If the Examiner believes that a telephone conference would be useful in moving the Application forward to allowance, the Examiner is encouraged to contact the undersigned at (310) 207-3800.

Respectfully submitted,

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on: October 15, 2001.

Lillian E. Rodriguez 10-15-01

Lillian E. Rodriguez October 15, 2001

MARKED-UP VERSION OF THE CLAIMS

IN THE CLAIMS

8. (Three Times Amended) A transistor device having a gate electrode overlying a gate dielectric formed directly on a semiconductor substrate, the gate dielectric comprising:

a first dielectric material having a first dielectric constant; [and]

a second dielectric material having a second dielectric constant different from the first dielectric constant[.]; and

the first and second dielectric materials being scaled for a technology.

9. The transistor of claim 8, wherein the second dielectric of the gate dielectric has a dielectric constant greater than the first dielectric constant.

10. The transistor of claim 8, wherein the first material of the gate dielectric has a first thickness and the second material of the gate dielectric has a second thickness, the combination of the first thickness and the second thickness defining a total thickness less than one-third of the length of the transistor gate.

11. The transistor of claim 8, wherein the first material thickness and the second material thickness are determined by the relationship

$$t_1/k_1 + t_2/k_2 = t_{ox}/k_{ox}$$

wherein t_1 is the first material thickness,

t_2 is the second material thickness,

t_{ox} is the minimum thickness for a gate dielectric of silicon dioxide for a chosen gate length,

k_1 is the dielectric constant for the first dielectric material,

k_2 is the dielectric constant for the second dielectric material, and

k_{ox} is the dielectric constant of silicon dioxide.

12. (Amended) The transistor of claim 8, wherein the first gate dielectric material is selected from one of [silicon nitride,] HfO_2 and ZrO_2.

13. The gate dielectric of claim 8, wherein the second dielectric material is selected from one of BST and PZT.

14. The gate dielectric of claim 8, further comprising a third dielectric material having a third dielectric constant.

15. (Twice Amended) An apparatus comprising:

a semiconductor substrate having a transistor device formed thereon, the transistor device having a gate dielectric disposed directly between a surface of the substrate and a gate electrode comprising:

a first dielectric material having a first dielectric constant; [and]

a second dielectric material having a second dielectric constant different from the first dielectric constant[.]; and

the first and second dielectrical materials being scaled for a technology.

16. The apparatus of claim 15, wherein the second dielectric constant is greater than the first dielectric constant.

17. The apparatus of claim 15, wherein the first material has a first thickness and the second material has a second thickness, the combination of the first thickness and the second thickness defining a total thickness less than one-third of the length of a transistor gate adapted to overly the gate dielectric.

18. The apparatus of claim 15, wherein the first material thickness and the second material thickness are determined by the relationship

$$t_1/k_1 + t_2/k_2 = t_{ox}/k_{ox}$$

wherein t_1 is the first material thickness,

t_2 is the second material thickness,

t_{ox} is the minimum thickness for a gate dielectric of silicon dioxide for a chosen gate length,

k_1 is the dielectric constant for the first dielectric material,

k_2 is the dielectric constant for the second dielectric material, and

k_{ox} is the dielectric constant of silicon dioxide.

19. (Amended) The apparatus of claim 15, wherein the first gate dielectric material is selected from one of [silicon nitride,] HfO_2, BaO, La_2O_3, Y_2O_3, and ZrO_2.

20. The apparatus of claim 15, wherein the second dielectric material is selected from one of BST and PZT.

21. The apparatus of claim 15, further comprising a third dielectric material having a third dielectric constant.